

Centre for Development of Advanced Computing

(Scientific Society of the Ministry of Electronics and Information Technology, Government of India)

CERTIFICATE

This is to certify that

Shashank Jain

has completed 900-hour full time Post Graduate Diploma course offered by

C-DAC's Advanced Computing Training School, Pune

This course has the following compulsory modules

- Advanced Digital Design
- ♦ System Architecture
- ◆ CMOS VLSI design and aspect of ASIC design
- ♦ HDL Simulation and Synthesis
- ♦ Verilog HDL, System Verilog, Linux Shell Scripting & Python
- ♦ Programming Fundamentals for Design and Verification
- ♦ General Aptitude & Communication
- Verification using UVM
- ◆ Project

This course was conducted during the period March 05, 2024 to August 19, 2024. Shashank Jain has been examined and found proficient in the above modules and has been conferred

PG Diploma in VLSI Design

with Grade B.

Grade Scale : A+ >=85%, A >=70% to <85%, B >=60% to <70%, C >=50% to <60%, D >=40% to <50%, F <40% to <50%, E >=50% to <60%, D >=40% to <50%, E <40% to <50%, E <40% to <50%, D >=40% to <50%, E <40% to <50% to <50%, E <40% to <50% to <50% to <50% to <50%, E <40% to <50% to <50%

Col. A. K. Nath (Retd.)

Executive Director

C-DAC, Pune

Gaur Sunder
Scientist 'F'
HoD ACTS, C-DAC, Pune

Risha P. R.
Associate Director
ACTS, C-DAC, Pune

B362412

Date : August 19, 2024



Place : Pune

Centre for Development of Advanced Computing (Scientific Society of the Ministry of Electronics and Information Technology, Government of India)



PG Diploma in VLSI Design

PERFORMANCE STATEMENT

(Duration: March 05, 2024 to August 19, 2024)

Name of the Student: Shashank Jain

Name of the Centre: C-DAC's Advanced Computing Training School, Pune

Sr. No	Name of the Module	Maximum Marks	Marks Scored
1.	Advanced Digital Design	50	29
2.	System Architecture	50	27
3.	CMOS VLSI design and aspect of ASIC design	100	67
4.	HDL Simulation and Synthesis	100	55
5.	Verilog HDL	100	67
6.	Programming Fundamentals for Design and Verification, Linux Shell Scripting & Python	100	69
7.	Verification using UVM	100	65
8.	System Verilog	100	59
	TOTAL	700	438

Marks Distribution: Theory 40%, Lab 40% and Internal 20%.

Result: Pass Grand Total: 438 / 700 Percentage: 62.57 % Grade: B

Shashank Jain has been awarded Grade A for Project Work, Grade C for General Aptitude & Communication.

Grade Scale: A+>=85%, A>=70% to <85%, B>=60% to <70%, C>=50% to <60%, D>=40% to <50%, F <40%

Gaur Sunder Scientist 'F'

HoD ACTS, C-DAC, Pune

Risha P. R. Associate Director ACTS, C-DAC, Pune

Place : Pune

M303500

Date : August 19, 2024

